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(54) Improved magnetoresistors.

(57) A magnetoresistive sensor that includes a very thin film of monocrystalline semi-conductive material, preferably having a band gap of at least about 0.35 electron volts. The device includes means for inducing or enhancing an accumulation layer adjacent the film outer surface. With film thicknesses below 5 micrometres, preferably below 3 micrometres, the presence of the accumulation layer can have a very noticeable effect. The unexpected improvement provides a significant apparent increase in mobility and conductivity of the semi-conductive material, and an actual increase in magnetic sensitivity and temperature insensitivity. A method for making the sensor is also described.

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IMPROVED MAGNETORESISTOR

Co-pending Patent Applications

This patent application is related to the following concurrently filed European patent applications Numbers , which are based on the following earlier filed United States patent applications USSN 229,396, USSN 289,634 and USSN 289,641.

Field of the Invention

This invention relates to magnetic field sensors as specified in the preamble of claim 1, for example as described by S.Kataoka in "Recent development of Magnetoresistive Devices and Applications", Circulars of Electrotechnical Laboratory No.182, Agency of Industrial Science and Technology, Tokyo (December 1974), and more particularly to improved thin film magnetoresistors and to methods of making such a magnetoresistor.

Background of the Invention

In the past, magnetoresistors were believed to be best formed from high carrier mobility semiconductive material in order to get the highest magnetic sensitivity. Hence, the focus was on making magnetoresistors from bulk materials that were thinned down or on films having sufficient thickness to exhibit a high average mobility.

A sensor in accordance with the present invention is characterised by the features specified in the characterising portion of claim 1.

The inventors have found a new way to approach making magnetoresistors. The inventors have found that if an accumulation layer is induced in the surface of an extremely thin film of semi-conductive material, the properties of the accumulation layer relevant to magnetic sensitivity can dominate over those of the remainder of the film.

Such accumulation layers can make higher band gap semi-conductor materials useful in magnetosensors. Such materials can be used at higher operating temperatures than lower band gap semi-conductive material, such as indium antimonide. However, it may even enhance the sensitivity of indium antimonide enough to allow it to be used at higher temperatures.

Summary of the Invention

From the foregoing, it is apparent that this invention involves a magnetoresistor formed in a film having an accumulation layer of current carriers, and in which the magnetic change in conductivity of the accumulation layer is not masked by conductivity of the balance of the film. The accumulation layer can be of the same conductivity type as that of the film or of opposite conductivity type. An opposite conductivity type accumulation layer is also referred to as an inversion layer but is considered to be within the scope of the phrase "accumulation layer" as used in this patent application.

This invention is especially directed to use of an accumulation layer in magnetoresistors made of higher band gap semi-conductive materials. However, it is expected to be beneficial in magnetoresistors made of still other semi-conductive materials.

This invention also provides new magnetoresistor constructions and methods of making magnetoresistors.

Description of the Drawings

Figure 1A is a schematic view of a magnetoresistor, showing its electrical current flow lines when no magnetic field is applied to it.

Figure 1B is a schematic view of a magnetoresistor, showing how the electrical current flow lines shown in Figure 1A are re-directed in the plane of a major surface of the magnetoresistor when a magnetic

field is applied perpendicular to that surface.

Figure 2 is an isometric view showing a magnetoresistor having two integral sensing areas electrically in parallel.

Figure 3 is a three-dimensional or contour plot showing the change of electrical resistance in a single element larger band gap semi-conductor magnetoresistor with changes in temperature and magnetic field strength.

Figure 4 is a two-dimensional plot of the fractional magnetoresistance over a wider temperature range than shown in Figure 3.

Figure 5 is a two-dimensional plot showing change in resistance with no magnetic field applied over a wider temperature range than shown in Figure 3.

Figure 6 is an elevational view showing a semi-conductor film in a pattern for providing a series-connected plurality of sensing areas integrated in a single magnetoresistor.

Figure 7A is an elevational view showing a metallization pattern for superposition on the Figure 6 pattern.

Figure 7B is an elevational view showing the Figure 7A metallization pattern superimposed on the Figure 6 semi-conductor pattern to delineate the plurality of sensing areas.

Figure 8 is a three-dimensional or contour plot showing the change of electrical resistance of a multiple sensing area magnetoresistor such as shown in Figure 7B.

Figures 9 and 10 are two-dimensional electron energy to depth plots showing how electrons could be confined in an accumulation layer under special layers on a surface of the sensing area of the magnetoresistor.

Figures 11A, 11B, and 11C are schematic views showing a magnetoresistor having a gate electrode over each of a plurality of sensing areas to electrically induce an accumulation layer in each sensing area. In Figures 11B and 11C, the gate electrodes are electrically biased internally, by two different techniques.

Figure 12 is a schematic view showing a magnetoresistor having accumulation layers not only in the sensing areas but also as conductors making electrical contact to the edges of the sensing areas.

Description of the Preferred Embodiments

A typical magnetoresistor element consists of a slab of semiconductor, typically rectangular in shape, through which a current is passed. Such a magneto resistor is described by S. Kataoka in "Recent development of Magnetoresistive Devices and Applications," Circulars of Electrotechnical Laboratory No. 182, Agency of Industrial Science and Technology, Tokyo (December 1974).

In the absence of a magnetic field, the current lines go from one injecting electrode to the other in parallel lines (see Figure 1A). This flow is between electrodes along the top and bottom edges of the rectangle in Figure 1A. The configuration (a rectangle in this example) is chosen so that an applied magnetic field, perpendicular to the slab, increases the current line trajectory (see Figure 1B). The magnetic field perpendicular to the plane of the rectangle thus lengthens the current flow lines. The longer length leads to higher electrical resistance, so long as the resulting lateral voltage difference is electrically shorted, as shown, by the top and bottom edge electrodes.

The best configuration for this effect to occur is one where the current injecting electrodes are along the longest side of the rectangle, and the ratio of this dimension ("width") to the shortest dimension ("length") is as large as possible. For the present invention, the length of the short edges of the rectangular sensing area is preferably about 30% to 50% of the length of the long edges of the rectangular sensing area. Such an optimal device configuration hence leads to a very low resistance. Kataoka teaches that the magnetic field sensitivity of such devices is best when the devices are made out of semi-conductors with as large a carrier mobility as possible. The resistivity of such devices is made less temperature-dependent when the semi-conductor material contains a large donor concentration, giving a large carrier density. These last two constraints imply that semi-conductors with high electrical conductivity are best suited for practical applications.

Combined with the geometrical restrictions described earlier, one can deduce that the final magnetoresistor element will have a low resistance. This has a practical drawback. Under a constant voltage, the power dissipated by the device is proportional to the inverse of the resistance. To limit ohmic heating (which would limit the operational temperature range of the sensor, if not destroy the sensor itself) whilst maintaining a large voltage output during sensor interrogation, it is desirable that a magnetoresistive element have a resistance around 1kW. The inventors consider this to typically be equivalent to a resistance of about 300W-3kW. A number of ways have been proposed to achieve such resistances. For example, as Kataoka has pointed out, one can put a number of elementary devices in series. Making a

plurality of sensing areas as integral parts of a single element is shown in Figure 2. Whilst only two sensing areas (i.e., devices) are shown, one could make an element with tens or hundreds of integral sensing areas (i.e., devices).

If the metal-semi-conductor (magnetic-field independent) interfacial contact resistance of one such elementary device is an appreciable fraction of the semi-conductor resistance of this elementary device, it will lower the sensitivity to a magnetic field. Thus, metals must be deposited which have a very low metal-semi-conductor interfacial contact resistance to avoid this sensitivity degradation. In most cases it would be preferable that the interfacial contact resistance between the sensing area and its electrodes be 10-100 times less than the resistance of the sensing area between those electrodes. Another option which alleviates the problem of low magnetoresistor device resistance has been to use active layers that are as thin as possible. This has been done by thinning wafers of indium antimonide (InSb), which were sliced from bulk ingots, down to thicknesses as small as 10 micrometres. The wafer thinning process is a very difficult process, since any residual damage from the thinning process will lower the electron mobility. Reducing electron mobility will decrease the sensitivity to a magnetic field of devices made from this material.

Another approach has been to deposit films of InSb onto an insulating substrate. On the other hand, in this latter case, the electron mobility of the resulting films is reduced to a fraction of that of bulk InSb. This reduction occurs because of defects in the film. With typical mobilities of 20,000 $cm^2V^{-1}sec^{-1}$, these films produce devices with greatly reduced sensitivity to a magnetic field compared to devices made from bulk InSb. The usual device structure for the prior magnetoresistors made from a film is schematically shown in Figure 2.

The great majority of the prior work until now has focused on InSb. This can be understood from the data in the following Table I.

TABLE I

Potential Magnetoresistor Materials at 300 ° K			
Semi-conductive Material	Maximum Electron Mobility	Crystal Lattice Constant	Energy Band Gap
	($cm^2V^{-1}sec^{-1}$)	(A)	(eV)
InSb	78,000	6.478	0.17
$Bi_{1-x}Sb_x$ (x<0.2)	32,000	6.429(Bi)	0-0.02
InAs	32,000	6.058	0.35
$In_{0.53}Ga_{0.47}As$ (on InP)	14,000	5.869	0.75
GaAs	8,000	5.654	1.4
GaSb	5,000	6.095	0.68
InP	4,500	5.869	1.27

Since the magnetoresistance effect is proportional to the square of the electron mobility for small magnetic fields, InSb is highly preferable. However, the difficulty of growing compound semi-conductors in general, and the fact that there is no suitable, lattice-matched, insulating substrate upon which it may be grown led the inventors to try growing Bi films. Such work has been previously reported by Partin et al. in Physical Reviews B, 38, 3818-3824 (1988) and by Heremans et al. in Physical Reviews B, 38, 10280-10284 (1988). Although the inventors succeeded in growing the first epitaxial Bi thin films, with mobilities as high as 25,000 cm^2V^{-1} sec^{-1} at 300 ° K (and 27,000 $cm^2V^{-1}sec^{-1}$ for $Bi_{1-x}Sb_x$ at 300 ° K), magnetoresistors made from these films had very low sensitivities. Modelling studies which the inventors have just completed indicate that this is to their knowledge an unrecognized effect of the fact that the energy band structure of Bi has several degenerate conduction band minima. Other high-mobility materials shown in Table I have a single, non-degenerate conduction band minimum. The inventors then began growing InSb thin films (on semi-insulating GaAs substrates) using the metal organic chemical vapor deposition (MOCVD) growth technique. After many months of effort, the inventors could only produce films with electron mobilities of 5,000 $cm^2V^{-1}sec^{-1}$.

The inventors then tried growing Indium Arsenide (InAs) on semi-insulating GaAs, and also on semi-insulating InP substrates. By "semi-insulating" is meant substrates of such high resistivity that they can be considered as substantially insulating. These latter substrates were made semi-insulating by doping them with Fe. They were tried in addition to GaAs because there is less lattice mismatch with InAs (see Table I).

After some time, the inventors were able to produce InAs films with a room temperature mobility of 13,000 $cm^2V^{-1}sec^{-1}$ on InP substrates, and of lower mobility on GaAs substrates. The better InAs films were formed by the following process.

An MOCVD reactor manufactured by Emcore Corporation, U.S.A. was used. InP substrates were heated to the growth temperature in an atmosphere of 5333 Pa (40 torr) of high purity (palladium-diffused) hydrogen to which a moderate quantity of arsine was added (80 SCCM, or standard cubic centimetres per minute). This produced about 0.02 mole fraction of arsine. The arsine was used to retard thermal decomposition of the InP surface caused by loss of the more volatile phosphorus. The way in which arsine reduces the surface roughening during this process is not well understood. Phosphine would have been preferred, but was not available at the time in the reactor. After reaching a temperature of 600° C, the arsine flow was reduced to 7 SCCM, and ethyl-dimethyl indium (EDMIn) was introduced into the growth chamber by bubbling high purity hydrogen (100 SCCM) through EDMIn which was held at 40° C. Higher or lower arsine flows during growth gave lower mobilities and worse surface morphologies. After 2.5 hours of InAs growth time, the EDMIn flow to the growth chamber was stopped and the samples were cooled to room temperature in an arsine-rich atmosphere (as during heat-up).

The thickness of the resulting InAs film was 2.3 micrometres. From conventional Hall effect measurements at 300° K, the electron density was $1.4x10^{16}$ cm^{-3} and the electron mobility was 13,000 $cm^2V^{-1}sec^{-1}$. These are effectively averages since the electron density and mobility may vary within a film. The film was not intentionally doped. Even though this is a very disappointing mobility, a crude magnetoresistor was made, since this required very little effort. A rectangular sample was cleaved from the growth and In metal was hand-soldered along two opposing edges of the sample, and leads were connected to the Inmetal. The length, which is the vertical dimension in Figures 1A and 1B, was 2 mm and the width, which was the horizontal dimension in Figures 1A and 1B, was 5 mm.

As expected, the resistance of the device was low (about 50 W) since the inventors did not have many elements in series. However, the magnetoresistance effect was large. It is shown in Figure 3. Furthermore, the device resistance and magnetoresistance were surprisingly stable with temperature in the range shown in Figure 3, which is -50° C to +100° C. A second, similar device was tested less thoroughly at temperatures as high as +230° C. The results of this latter testing are shown in Figures 4 and 5. In Figure 4, the applied magnetic field was 0.4 Tesla. The fractional magnetoresistance is plotted as a function of temperature between B = 0.4 Tesla and B = 0. Despite the fact that the indium metal used for contacts has a melting point of 156° C, the magnetoresistor still functioned very surprisingly well at 230° C, with the fractional increase in resistance for a given magnetic field (0.4 Tesla) reduced by less than one half compared to the response near room temperature (as shown in Figure 4).

The device resistance in zero magnetic field, R(0), decreased over the same temperature range by a factor of 5 (as shown in Figure 5). The inventors also found this to be surprisingly good, even taking into account the relatively large energy gap of InAs.

The inventors own detailed analysis of transport data from these films suggests that there are current carriers with two different mobilities present. In retrospect, it looks like the results are related to an accumulation layer of electrons at the surface of the sensing layer. The inventors have now found that Wieder has reported in Appl. Phys. Letters, 25, 206 (1974) that such an accumulation layer exists just inside the InAs near the air/InAs interface. It appears to the inventors that there are some errors in the Wieder report. However, the inventors think that the basic conclusion that an electron accumulation layer exists is correct. These electrons are spatially separated from the positive charge at the air/InAs interface. Thus, they are scattered relatively little by this charge, resulting in a higher mobility than would normally be the case. They also exist in a very high density in such an accumulation layer, so that, as the temperature increases, the density of thermally-generated carriers is a relatively small fraction of the density in the accumulation layer. This helps stabilize the resistance (at zero magnetic field) with temperature. Thus, it appears that the relatively low measured electron mobility of 13,000 $cm^2V^{-1}sec^{-1}$ is an average for electrons in the accumulation layer and for those in the remainder of the thickness of the film.

Thus, normally one would want to grow a relatively thick layer of InAs to make a good magnetoresistor, since crystal quality (and mobility) generally improve with thickness when growing on a lattice-mismatched substrate. However, the thicker the layer becomes, the greater its conductivity becomes and the less apparent the benefits or presence of a surface accumulation layer would be. Thus, the inventors' current understanding of their devices suggests that relatively thinner layers are preferable, even if the average film mobility decreases somewhat, since this will make the conductivity of the surface accumulation layer a greater fraction of the total film conductivity. In a preferred method of making such a sensor using an indium phosphate substrate, a metal organic chemical vapor technique is used to deposit a nominally undoped monocrystalline film of indium arsenide onto said substrate to a thickness of less than 5

micrometres. Preferably this preferred method also includes exposing said deposited film to air. The exact relationships between film thickness, crystal quality and properties of the surface accumulation layer are currently under study.

The inventors have since made multi-element magnetoresistors from this material using Au (or Sn) metallization. Such multi-element magnetoresistors usually contain over ten discrete sensing areas. First, conventional photolithography techniques were used to etch away unwanted areas of an Indium Arsenide (InAs) film from the surface of the Indium Phosphide (InP) substrate to delineate the pattern shown in Figure 6. A dilute solution (0.5%) of bromine in methanol was used to etch the InAs. Then, a blanket layer of Au metallization 100 nanometres (1000 Angstroms) thick was deposited using conventional vacuum evaporation techniques over the entire surface of the sample, after removing the photoresist. Conventional photolithography was then used to etch away unwanted areas of the Au film to delineate the gold pattern shown in Figure 7A. A dilute aqueous solution of KCN was used for this step. (The inventors think dissolved oxygen is helpful, which can diffuse into the solution from ambient air or be supplied in the form of a very small addition of hydrogen peroxide.) The resultant composite of the two patterns, with the gold pattern overlying the InAs film pattern, is shown in Figure 7B.

Leads were then attached by silver epoxy resin to the large Au end bonding pads. Leads could also be attached by normal and accepted filamentary wire-bonding techniques. If so, and especially if a modern wire-bonding apparatus were used, the bonding pads could easily be made much smaller. Also, many devices such as shown in Figures 6,7A and 7B could be made simultaneously using conventional integrated circuit technology. The resulting devices typically have a resistance near 1 KW (typically + or - 20%) at room temperature in zero magnetic field. Surprisingly, the magnetoresistance effect on the multi-sensing area device was much larger than the effect on a single sensing area device. For comparison, of these effects at a given magnetic field, see Figures 8 and 3. In the multi-element device (i.e., plural sensing area element), the sensing areas had a length to width ratio of 2/5. The inventors do not understand why the multi-element device works better since the length to width ratio of each element is 2/5, the same as for the single element device characterized in Figure 3, which was fabricated using part of the same InAs grown layer. Another multi-element magnetoresistor was made similarly to the one just described, but with a length to width ratio of 4/5. It had nearly as large a magnetoresistance as the one made according to the patterns in Figures 6, 7A and 7B. Again, the inventors do not yet understand this, but the resulting devices work very well. Even a device with a length to width ratio of 6/5 works well.

The relative stability of these magnetoresistors with temperature also now appears to be increasingly important, since some automotive applications require operation from -50 °C to as high as +170 °C to +200 °C, and there are known applications requiring even higher temperatures (to 300 °C). There is reason to believe that the present invention will provide magnetoresistors operating at temperatures as high as 300 °C, and even higher.

A potential problem with InAs magnetoresistors made in accordance with this invention is the potential importance of the air/InAs interface, which might cause the device characteristics to be sensitive to changes in the composition of ambient air, or cause the characteristics to slowly change with time or thermal history because of continued oxidation of the surface. A preferred sensor according to this invention is one in which there is a protective but gas-permeable coating over each sensing area of the sensor. Preferably such a coating is permeable to ambient air. The inventors have tried coating the surfaces of two devices with a particular epoxy resin made by Emerson and Cuming, a division of Grace Co. U.S.A. The epoxy resin used was "Stycast", number 1267. Parts A and B were mixed, applied to the devices, and cured at 70 °C for two hours. The inventors did not observe any significant changes in the device characteristics at room temperature as a result of this encapsulation process. The inventors have not yet systematically tested these devices at other temperatures, but they are encouraged by this preliminary result. The inventors think other forms of encapsulants need to be explored, such as other epoxy resins and thin film dielectrics, such as SiO_2 or Si_3N_4.

In order to still have a very low metal-semi-conductor contact resistance between the InAs and the contact and shorting bar metallization, it may be necessary to modify the processing sequence previously described in connection with Figures 6, 7A and 7B. For example, with an inverse of the mask contemplated in the previous discussion, the photoresist on the surface could then be used as a mask for wet-etching (e.g., by wet chemicals or reactive ions, or ion beams) of the dielectric or high energy gap semi-conductor layer to expose the InAs. Au or other metals could then be deposited by vacuum evaporation (or by other conventional processes, such as sputtering, or electroplating) and then the photoresist could be removed, resulting in lift-off of the undesired regions of metal. Alternatively, after etching through to the InAs, the photoresist could be removed, Au or other metal could be deposited uniformly across the surface, and then, after deposition of photoresist, the mask pattern in Figure 7A could be aligned with the pattern etched into

the dielectric and the Au could be patterned as before.

As an additional alternative, if a sufficiently thin layer (e.g., 20 nanometres (200 Angstroms)) of high energy gap semi-conductor is present, the original processing sequence described could be modified by deposition of a low-melting- temperature eutectic alloy, such as Au-Ge, Au-Ge-Ni,or Ag-Sn, in place of Au. After patterning similarly to the way the Au was patterned (or using the inverse of the mask in Figure 7 and lift-off), the sample is heated to a moderate temperature, typically to somewhere in the range of 360° C to 500° C for Au-Ge-based alloys, thus allowing the liquid metal to locally dissolve the thin layer of high energy gap semi-conductor, effectively contacting the InAs.

In the most recent work, the inventors have changed the InAs growth procedures somewhat. The procedures are the same as before, but the InP wafer is heated to 460° C in a larger arsine mole fraction (0.1). After 0.5 minutes at 460° C, during which the native oxide on InP is believed to desorb, the temperature is lowered to 400° C and 20 nanometres (200 Angstroms) of InAs in thickness is grown. The temperature is then raised to the growth temperature of 625° C (with the arsine mole fraction still 0.1), and then EDMIn is introduced while the arsine flow is abruptly reduced to 5 SCCM (about 0.001 mole fraction). The EDMIn is kept at 50° C, and the high purity hydrogen is kept bubbling through it at a rate of 75 SCCM. Again, the arsine flow of 5 SCCM seems near-optimal for these growth conditions. The resulting films have somewhat enhanced sensitivity to a magnetic field relative to those grown earlier.

Whilst all of the recent work has concentrated on magnetoresistors fabricated from InAs films on semi-insulating (i.e., substantially electrically insulating) InP substrates, the inventors think that a more mature growth capability will permit films of InAs with nearly comparable quality to be grown on semi-insulating GaAs substrates as well. In either case, other growth techniques such as molecular beam epitaxy, liquid phase epitaxy or chloride-transport vapor phase epitaxy may also prove useful.

The above-mentioned Indium Arsenide (InAs) thin film devices, fabrication processes, and operating characteristics are described and claimed in a separate European patent application Number based on USSN 289,634, that is being simultaneously filed with this patent application.

On the other hand, the inventors think that the presence of what may be a naturally-occurring accumulation layer in the above-mentioned thin film InAs magnetoresistors is what makes them work so well, and which enables production of a practical device. The inventors believe that this fundamental concept is new to magnetoresistors, and that this concept can be expanded in a multiplicity of ways, not only to Indium Arsenide but to other semi-conductive materials as well. In this patent application is further described and claimed a variety of techniques by which an accumulation layer can be induced in the semi-conductor layer, by other than a natural occurrence or inherent occurrence as a result of the fabrication process.

The following discussion describes some of the other ways of inducing or enhancing an electron accumulation or inversion layer in InAs thin films and in other semi-conductive materials in thin film form, to attain effective high mobilities. There are three basic advantages to the use of strong electron accumulation layers in magnetoresistor active regions. It is repeated here that the term "electron accumulation layer", as used in this patent application is also intended to include electron inversion layers.

First, electron accumulation layers or strong electron inversion layers can contain a density of electrons significantly larger than the intrinsic density at any given temperature. This must improve the temperature stability, since the thermally-excited carriers are a small fraction of the accumulated or strongly inverted ones.

Second, accumulation layers enhance the mobility of the carriers in the semi-conductor. This effect has been experimentally observed in thin indium arsenide (InAs) films, especially at higher temperatures. They will enhance the sensitivity of the magnetoresistor. One possible cause of this effect may be that in such accumulated or strongly inverted layers large electron densities can be achieved without the presence of a large density of ionized impurities in the same spatial region, which would limit the carrier mobility. This effect is similar to the "modulation doping" of layers described by G. Burns in Solid State Physics, pp. 726-747, Academic Press (1985). Such an effect is used in the fabrication of High-Electron-Mobility-Transistors (HEMTs).

Third, accumulation or strong inversion layers are inherently close to the surface or interface of a semi-conductor. This makes it relatively easy to induce, enhance, or control these accumulation or strong inversion layers through the use of thin film structures deposited on top of the semi-conductor, possibly in combination with voltage biases.

Accumulation layers have been used in silicon MOSFET Hall plates, and are described by H.P. Baltes et al. in Proc. IEEE, 74, pp. 1107-1132, especially pp. 1116-7, (1986). In the MOSFET Hall effect devices, a biased gate electrode in a Metal-Oxide-Semi-conductor was used to generate a suitably thin electron layer close to the Semi-conductor-Oxide interface. Four electrodes were then used to contact that layer: a source

and a drain through which current is passed, and two intermediate electrodes across which the Hall voltage is generated. Further, Baltes et al. ibid. also describe a split-drain MOSFET using an accumulation-layer based sensor with only four electrodes (one source, two drains, and one gate). One of the virtues of a magnetoresistor over a Hall effect device is that the magnetoresistor has only two electrodes. In order to preserve this in the improved magnetoresistor concept of the present invention, the inventors propose to use, in conjunction with a magnetoresistor layout such as described in Figure 2, a number of new ways to generate accumulation or inversion layers without using externally-biased gate electrodes.

In a first embodiment, use is made of the fact that the natural interface between InAs and air is known to generate an electron accumulation layer in InAs. A similar effect may exist in InSb, and the technique may therefore be applicable to thin film magnetoresistors made with this semi-conductor material. The inventors would not, however, expect such devices to work as well as InAs at very high temperatures. The very small energy gap of InSb (see Table I) would cause thermal generation of carriers that would cause increased conductivity in the InSb film adjacent to the accumulation layer, making the conductivity of the accumulation layer a relatively small fraction of the total device conductivity. Thus, the benefits of the accumulation layer would be lost at a lower temperature in InSb than in the higher energy band gap InAs. The inventors experimentally grew a 2.3 micrometre thick epitaxial layer of InAs on an insulating InP substrate using Metal Organic Chemical Vapor Deposition (MOCVD). Hall and magnetoresistance measurements on the layer in the temperature range of 350° K to 0.5° K, and in magnetic fields up to 7 Tesla reveal the presence of at least two "types" of carriers, in roughly equal concentrations, but with very different mobilities (by a factor of 2 to 3). In retrospective view of the afore-mentioned Wieder publication, it is reasonable to assume that one of them is the accumulation layer located near the air interface. The inventors built two 2 mm long, 5 mm wide magnetoresistors out of this film which developed a very usable magnetic field sensitivity, whilst maintaining good temperature stability (see Figs.3, 4, and 5). The inventors believe it is possible to preserve this sensitivity after covering the InAs surface with a suitable encapsulating coating (e.g., an epoxy resin or other dielectric material).

In a second embodiment, a capping layer of a large-gap semi-conductor such as GaAs, InP, AlSb, or $In_{1-y}Al_yAs$ can be grown on top of the narrow-gap active layer semi-conductor (typically InAs or $In_{1-x}Ga_xAs$ with $0<x<0.5$, although a similar structure using InSb can be conceived). In this capping layer, the inventors put donor-type impurities, such as Si, Te, Se, or S. These will release an electron, which will end up in the layer where it has minimum energy, i.e., the narrow-gap semiconductor. This leaves a layer of positively ionized donor-impurities in the large-gap capping layer; but they are spatially removed from the electrons in the active layer, and hence do not significantly scatter them.

In a third embodiment, the inventors propose to deposit a layer of metal on top of the device active region with the purpose of creating a Schottky barrier. A plot of the electron energy levels adjacent the metal-semi-conductor interface in this third embodiment is shown in Figure 9. In referring to Figure 9, it can be seen that there will be a depletion of the top region of the active narrow-gap semi-conductor. If the active layer is thin enough (100-200 nanometres (1000-2000 Angstroms)), this will confine electrons in the active layer towards the substrate, resulting in electrical properties similar to those of an accumulation layer. Metals that generally form Schottky barriers to III-V compounds, such as Au or Al may be useful, although the inventors have not adequately studied this structure experimentally yet.

In a fourth embodiment, the inventors propose to deposit on the active layer of a narrow-gap semi-conductor a layer of large-gap semi-conductor, or of a dielectric such as SiO_2 or Si_3N_4, and on top of that a gate electrode. An electron energy plot going through the layers at the relevant interfaces is shown in Figure 10. The metal of the gate electrode in Figure 10 can be chosen such that it induces an accumulation region near the semi-conductor-dielectric interface, by effect of the difference between the electron affinity in the semi-conductor, and the work function in the metal. Conversely, a different metal with larger work function can be used to deplete the semi-conductor-dielectric interface and electrostatically confine the electrons near the substrate, much as in the third embodiment mentioned above.

In a fifth embodiment, it is suggested that the gate electrodes described in the fourth embodiment be biased so as to generate accumulation layers in the semi-conductor under them. Such a concept is schematically shown in Figures 11A, 11B, and 11C. In Figure 11A, it can be seen that, if desired, one could use one or more added contacts to separately bias the gate electrodes. This would not ordinarily be preferred but could be done. It would not be preferred because one of the advantages to a magnetoresistor resides in that it only has two contacts. It is only shown here for completeness. On the other hand, additional contacts are not actually necessary. The gate electrodes can be electrically biased by an internal resistor circuit, examples of which are shown in Figures 11B and 11C.

Reference is now specifically made to the fifth type of embodiments shown in Figures 11b and 11c. Since the gate leakage currents are very minimal, a very high resistance (>1MW) circuit can be used for

biasing. As a special case in Figure 11B, resistor R1 can be made extremely large (open-circuit), and the other resistors can all be made to have zero resistance (short-circuit). Thus, the full positive bias applied to one external electrode (relative to the other external electrode) is applied to all gates in this special case. An alternative is to connect the gates over each semi-conductor region with the shorting bar between two other semi-conductor regions located such that the potential difference between the gate (i.e., the shorting bar) and the active region induces an accumulation layer in the latter. This latter version of internal biasing of the gate electrodes is shown in Figure 11C. A special case of this configuration is one in which each gate is connected to the adjacent shorting bar. In this configuration, each element might be considered to be a MISFET transistor with gate and drain shorted.

In the five preceding embodiments, the accumulation layers were used only to enhance the desirable transport properties of the semi-conductor in the sensing area. The configuration of the magnetoresistor, i.e., the length over width ratio of each active element, was still defined by the use of metallic shorting bars. The structure of Figure 11B can be extended to define the configuration of the magnetoresistive elements themselves, by modulating the carrier density and hence the conductivity, inside the semi-conductor active layer. This forms a sixth embodiment of this invention. An example of such a structure is schematically shown in Figure 12. Again, an external (integrated into the chip) resistance network is used in this sixth embodiment to bias a succession of gate electrodes to create a series of strongly accumulated regions. These can be used instead of metallic shorting bars to create geometrical magnetoresistance. Such a structure could potentially be superior to one in which metallic shorting bars are used, because field-insensitive contact resistances between the metal and the semi-conductor would be eliminated.

Again, a special case can be considered for this sixth embodiment, as was considered in the fifth embodiment. In this special case of the sixth embodiment, the resistor R1 of Figure 12 is open-circuited and the other resistors (R2, R3 ...) are short-circuited, so that the entire positive bias applied to one external electrode is also applied to each gate. Thus, the natural accumulation layer normally present on an InAs surface would exist between the gates as in Figure 11A, but have a lower electron density. If desired, the gates could be biased negatively to eliminate the electron accumulation layers between the gates, or even to generate a strong inversion layer with carriers of the opposite type (holes). While the emphasis of this record of invention is on devices with only two external leads, the gates could be connected through a resistor network to a third external lead, making this version of the magnetic field sensor externally controllable through a voltage bias externally supplied to the gate lead. As hereinbefore indicated, a similar three terminal device could be made with the device shown in Figure 11A.

In a seventh embodiment, a lightly p-type film is grown (typically doped with Zn, Cd, Mg, Be, or C). In the case of InAs, the surface would, the inventors believe, still have a strongly degenerate electron layer, but it would be an inversion layer. Such an inversion layer would have a large electron density near the surface, and then a relatively thick (typically 0.1 mm to 1 mm or more, depending on dopant density) region of very low carrier density, similar to the space charge region of an n+/p junction. This might be advantageously used to reduce the conductivity of the film adjacent to the electron strong-inversion layer. At very high device operating temperatures, the intrinsic carrier density of narrow energy gap semi-conductors like InAs would tend to defeat this strategy somewhat, and other, higher energy gap semi-conductors such as $In_{1-x}Ga_xAs$ might be preferred (see Table I). $In_{0.53}Ga_{0.47}As$ is a special case, since it can be lattice-matched to semi-insulating InP substrates. This makes it easier to grow such films with high crystalline quality.

The acceptor dopants mentioned above (i,.e., Zn, Cd, Mg, Be, and C) have small activation energies in the III-V compounds of interest (see Table 1). However, there are other acceptor dopants with relatively large activation energies, such Fe, in $In_{0.53}Ga_{0.47}As$. This means that relatively large thermal energy is required to make the iron ionize and contribute a hole to conduction. However, the iron will compensate for a concentration of donor impurities frequently present in the material so that they do not contribute electrons to the conduction band. Thus, doping this material with iron will make it tend to have a high resistivity, except in the electron-rich accumulation layer. It would in this case be desirable to grow a thin undoped $In_{0.53}Ga_{0.47}As$ layer (e.g., 0.1 micrometre thick, after correcting for iron diffusion effects) on top of the iron-doped layer in order to obtain the highest possible electron mobility and density in the accumulation layer. It is recognized however, that finding suitable dopants with large activation energies may not be practical for smaller band gap semi-conductive materials. Furthermore, the other embodiments discussed above could also be used in conjunction with this one advantageously to reduce the conductivity of the film adjacent to the high electron density region.

The emphasis of the above discussion has been on electron accumulation or inversion layers. Hole accumulation or inversion layers could also be used. However, electrons are usually preferred as current carriers in magnetoresistors since they have higher mobilities in the materials shown in Table I.

power consumption of said sensor is significantly reduced but sensor size is not significantly increased.

14. A method of making a magnetoresistive sensor comprising the steps of: providing a substantially electrically insulating monocrystalline substrate; depositing a nominally undoped monocrystalline film of a substantially lattice-matching semi-conductive material onto said substrate to a thickness of less than 5 micrometres, using a metal organic chemical vapor deposition process; defining a rectangular magnetic field sensing area on said film; forming an elongated conductor along each long edge of said rectangular sensing area, whereby current carriers can be injected into said sensing area for detection of a magnetic field; and coating said sensing area with at least one layer for maintaining an accumulation layer induced in said film.

15. A method of making a magnetoresistive sensor according to claim 14, in which the substantially lattice-matching semi-conductive material is deposited onto said substrate to a thickness of less than 3 micrometres, said sem-conductive material has a band gap of at least about 0.35 electron volt and a given average carrier concentration and given average electron mobility; and said sensing area is coated with at least one layer for inducing or enhancing said accumulation layer in said sensing area of said film.

Fig.1a.

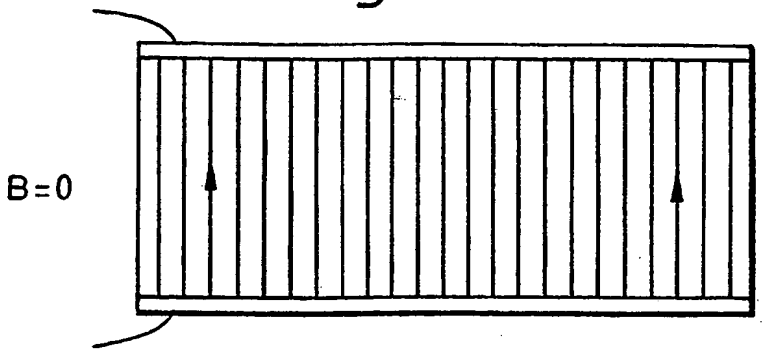


Fig.1b.

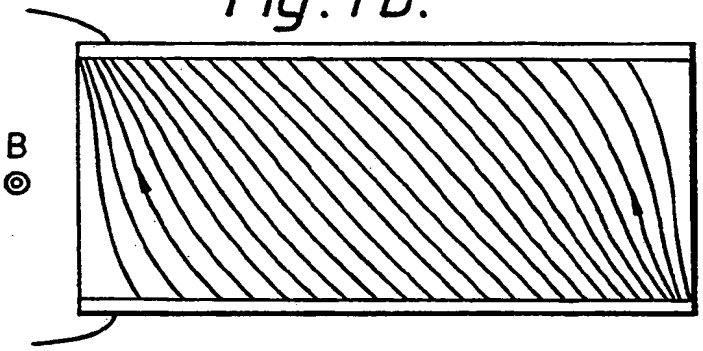
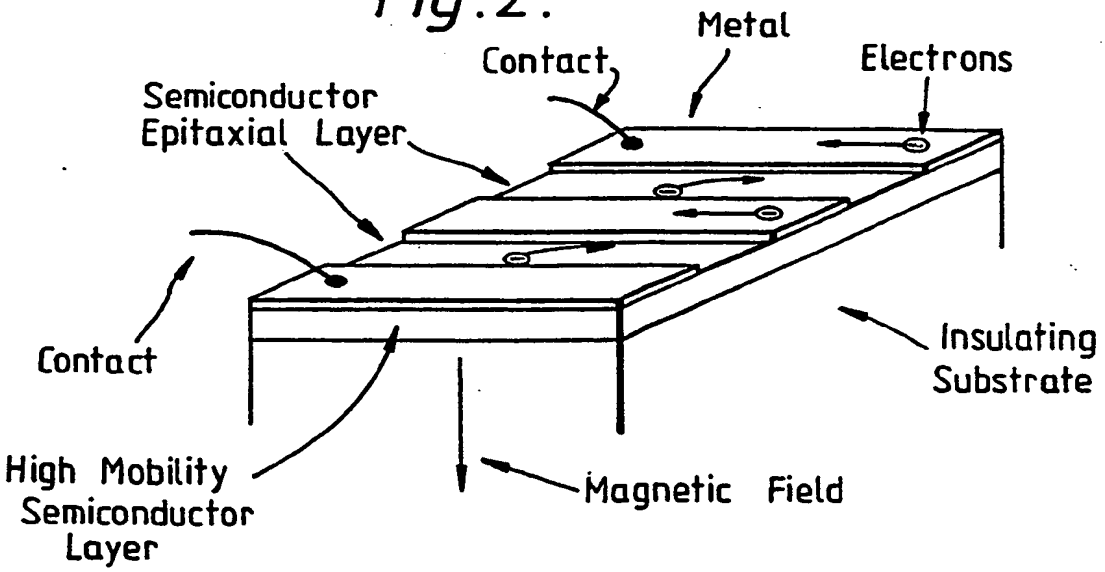


Fig.2.



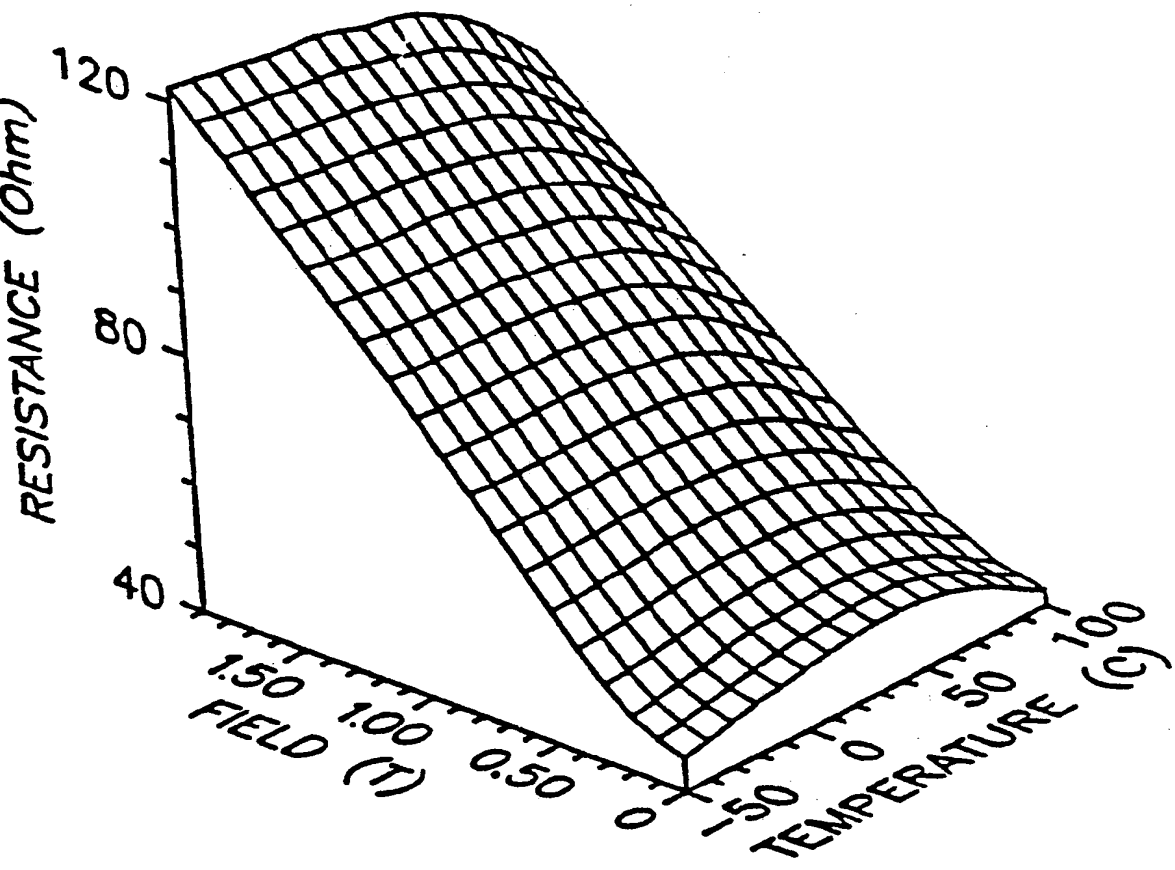


Fig. 3.

Fig.4.

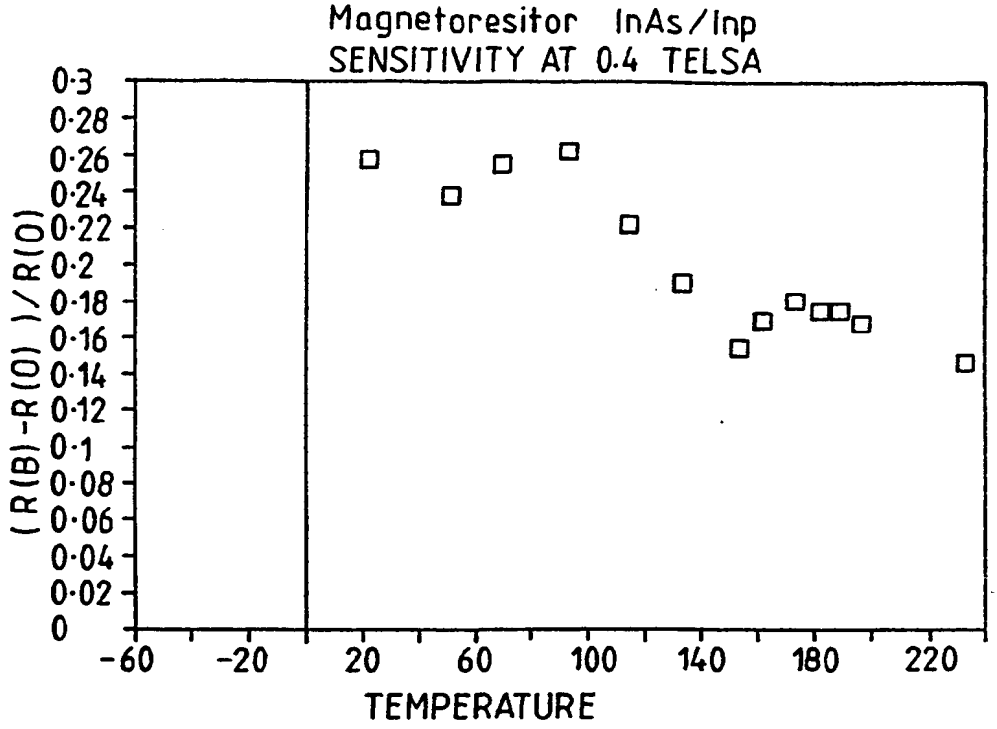

Magnetoresitor InAs/Inp
SENSITIVITY AT 0.4 TELSA
(R(B)-R(0))/R(0)
0·3
0·28
0·26
0·24
0·22
0·2
0·18
0·16
0·14
0·12
0·1
0·08
0·06
0·04
0·02
0
-60
-20
20
60
100
140
180
220
TEMPERATURE

Fig.5.

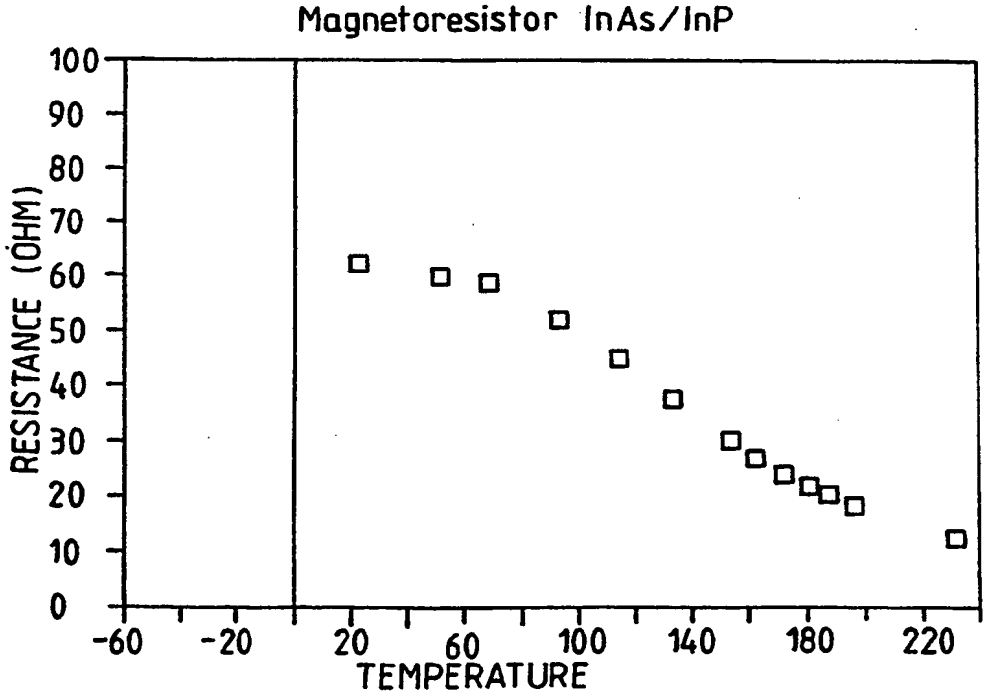

Magnetoresistor InAs/InP
RESISTANCE (OHM)
100
90
80
70
60
50
40
30
20
10
0
-60
-20
20
60
100
140
180
220
TEMPERATURE

Fig.6.

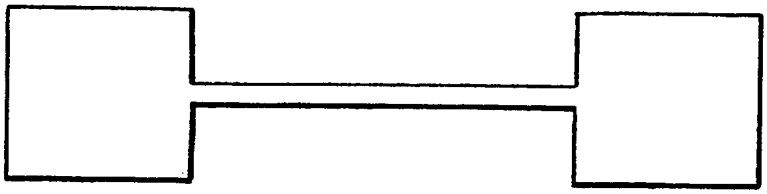


Fig.7a.

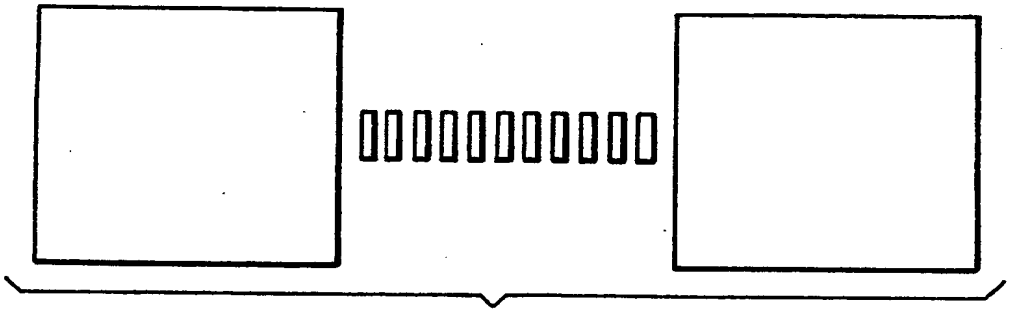
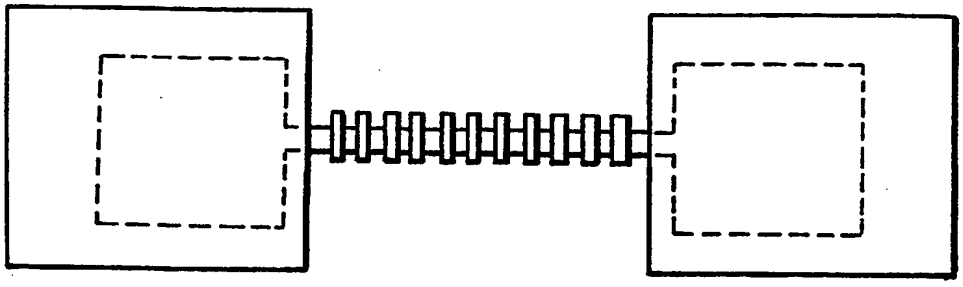


Fig.7b.



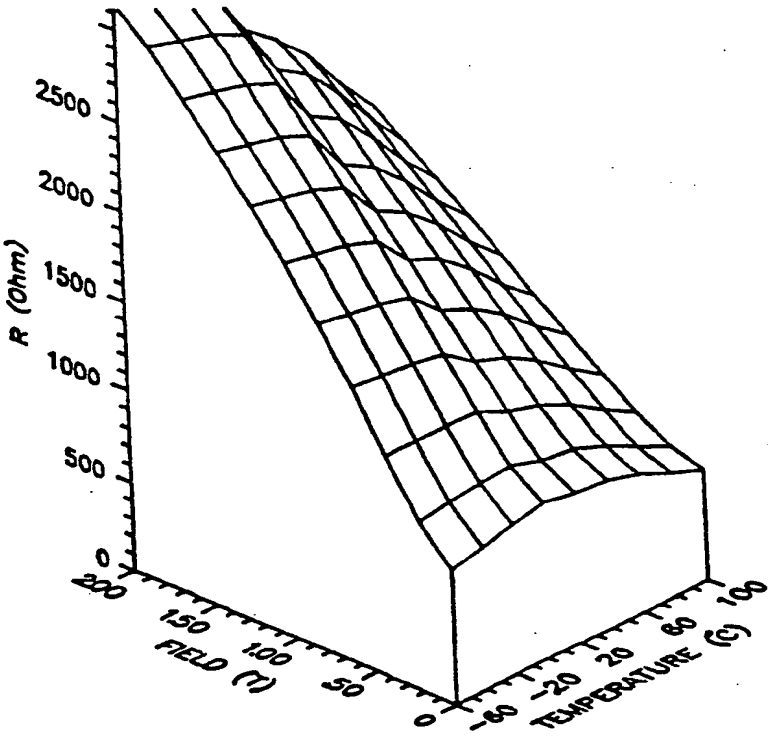


Fig. 8.

Fig. 9.

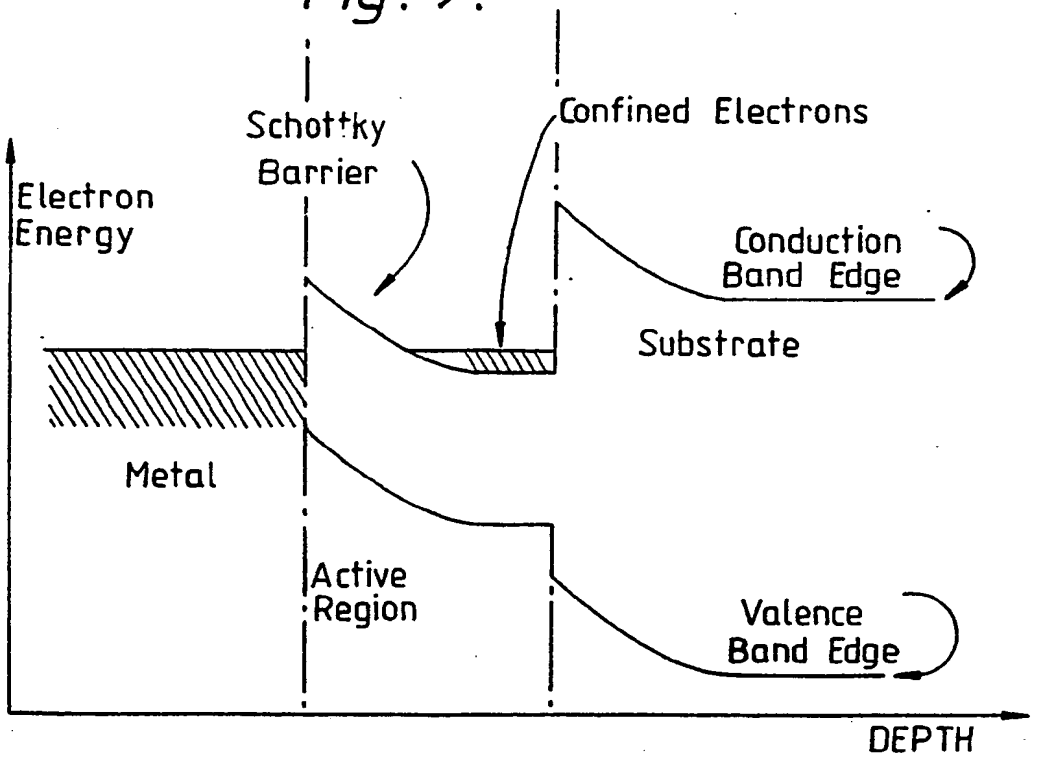


Fig. 10.

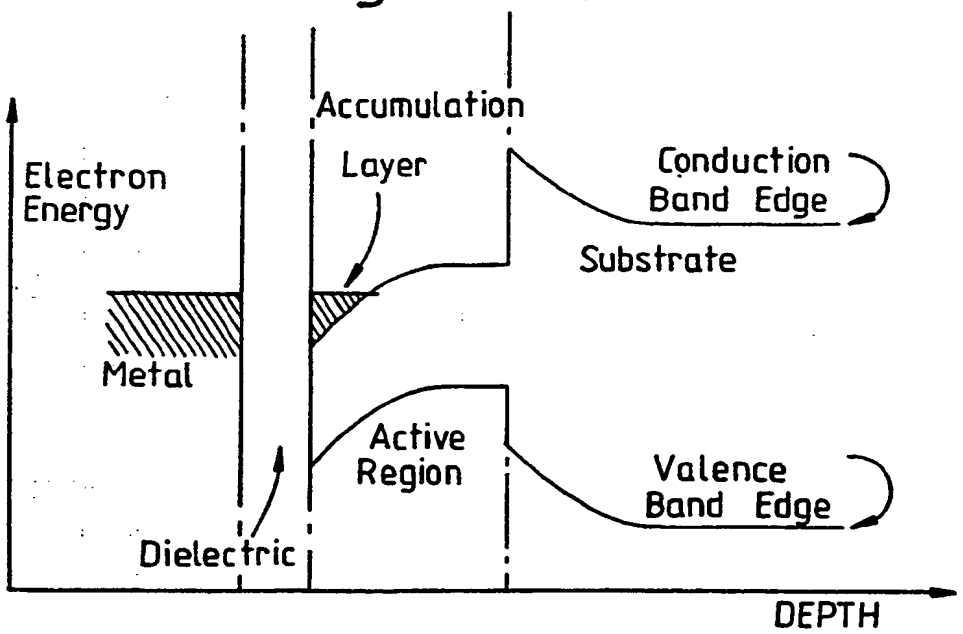


Fig.11a.

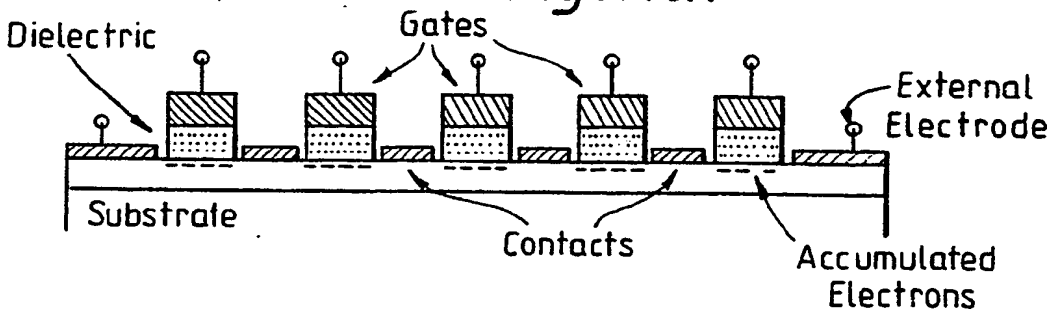


Fig.11b.

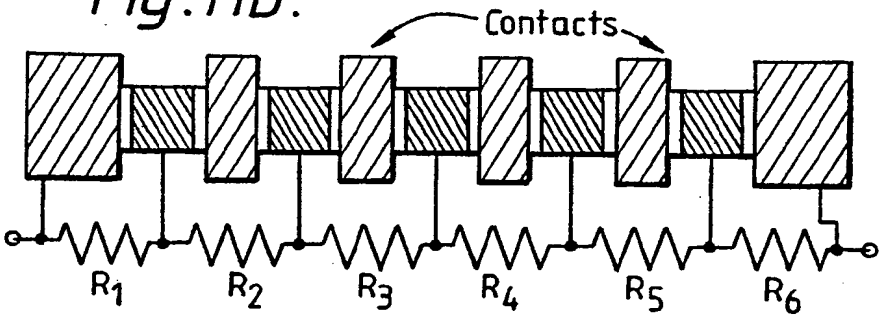


Fig.11c.

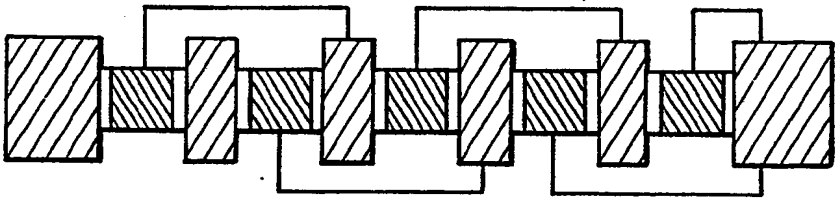
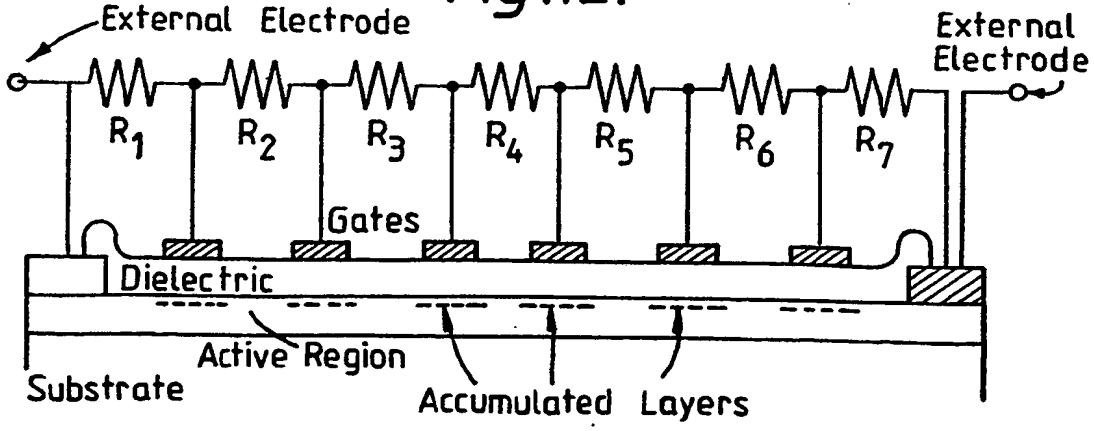


Fig.12.



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(54) Improved magnetoresistors.

(57) A magnetoresistive sensor that includes a very thin film of monocrystalline semi-conductive material, preferably having a band gap of at least about 0.35 electron volts. The device includes means for inducing or enhancing an accumulation layer adjacent the film outer surface. With film thicknesses below 5 micrometres, preferably below 3 micrometres, the presence of the accumulation layer can have a very noticeable effect. The unexpected improvement provides a significant apparent increase in mobility and conductivity of the semi-conductive material, and an actual increase in magnetic sensitivity and temperature insensitivity. A method for making the sensor is also described.

EP 0 375 107 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 89 30 7120

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	US-A-4568905 (PIONEER ELECTRONIC CORP.) * column 2, lines 1 - 14; figure 1 *	1	H01L43/08
A	US-A-3898359 (PRECISION ELECTRONIC COMPONENTS) * abstract; figure 4 *	2, 3	
A	ELECTRONICS & COMMUNICATIONS IN JAPAN, PART II - ELECTRONICS. vol. 71, no. 3, March 1988, NEW YORK US pages 110 - 115; Takashi Taguchi et al.: "AlGaAs/GaAS Heterojunction Hall Device" * the whole document *	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)
H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	08 OCTOBER 1990	PELSERS L.

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